CLAIMS

1. A metal interconnect layer for a semiconductor device, comprising:

a first upper portion having a first width; and

a second lower portion under the first upper portion, the second lower portion having a second width wider than the first width.

2. The metal interconnect layer of claim 1, wherein the metal interconnect layer comprises:

a barrier layer deposited along an interlevel dielectric (ILD) film with a trench having a lower width and an upper width, the lower width being wider than the upper width; and

a conductive layer deposited over the barrier layer, filling the trench, the conductive layer having a lower width and an upper width, the lower width being wider than the upper width.

3. The metal interconnect layer of claim 2, wherein the ILD film is formed of a single insulation layer with a material layer selected from the group consisting of undoped silicate glass (USG) layer, silicon oxide fluoride (SiOF) layer, tetraethylorthosilicate (TEOS) layer, spin-on glass (SOG) layer and borophosphosilicate glass (BPSG).

4. The metal interconnect layer of claim 3, wherein the thickness of an upper portion of the ILD film surrounding a portion of the trench with the upper width is in the range of 20-70% of the thickness of the entire ILD film.

5. The metal interconnect layer of claim 2, wherein the ILD film comprises first and second insulation layers deposited in sequence, the trench being formed in the ILD film such that the portion of the trench formed in the first insulation layer is wider than the portion of the trench formed in the second insulation layer.

6. The metal interconnect layer of claim 5, wherein the thickness of the second insulation layer is in the range of 20-70% of the thickness of the entire ILD film including the first and second insulation layers.

7. The metal interconnect layer of claim 5, wherein the second insulation layer is formed of layer selected from the group consisting of a USG layer, SiOF layer, TEOS layer, SOG layer and a BPSG layer; and the first insulation layer is formed of at least one of a flowable oxide (FOX) layer and a hydride organic siloxane polymer (HOSP) layer such that the first insulation layer has a higher etch rate than the second insulation layer.

8. The metal interconnect layer of claim 2, wherein the barrier layer is formed of one of a Ta layer, TaN layer, Ti layer, TiN layer, and a bilayer of these material layers.

9. The metal interconnect layer of claim 2, wherein the conductive layer is formed of one of a Cu and a W layer.

10. A metal interconnect layer for a semiconductor device, comprising:

a first upper portion having a first width;

a second middle portion having a second width; and

a third lower portion having a third width, the third width being wider than the first and second widths.

11. The metal interconnect layer of claim 10, wherein the metal interconnect layer comprises:

a barrier layer deposited along an interlevel dielectric (ILD) film with a trench having a lower width, a middle width and an upper width, the middle width being wider than the upper and lower widths; and

a conductive layer deposited over the barrier layer, filling the trench, the conductive layer having a lower width, a middle width and an upper width, the middle width being wider than the upper and lower widths.

12. The metal interconnect layer of claim 11, wherein the ILD film is formed as a single layer with a material layer selected from the group consisting of undoped silicate glass (USG) layer, silicon oxide fluoride (SiOF) layer, tetraethylorthosilicate (TEOS) layer, spin-on glass (SOG) layer and borophosphosilicate glass (BPSG) layer.

13. The metal interconnect layer of claim 12, wherein the thickness of a middle portion of the ILD film surrounding a portion of the trench with the wider middle width is in the range of 20-50% of the thickness of the entire ILD film.

14. The metal interconnect layer of claim 11, wherein the ILD film comprises first, second and third insulation layers deposited in sequence, the trench being formed in the ILD film such that the portion of the trench formed in the second insulation layer is wider than the portions formed in the first and third insulation layers.

15. The metal interconnect layer of claim 14, wherein the thickness of the second insulation layer is in the range of 20-50% of the thickness of the entire ILD film including the first, second and third insulation layers.

16. The metal interconnect layer of claim 14, wherein each of the first and third insulation layers is formed of at least one of a USG layer, SiOF layer, TEOS layer, SOG layer and a BPSG layer; and the second insulation layer is formed of at least one of a flowable oxide (FOX) layer and a hydride organic siloxane polymer (HOSP) layer having a higher etch rate than the first and third insulation layers.

17. The metal interconnect layer of claim 11, wherein the barrier layer is formed of at least one of a Ta layer, TaN layer, Ti layer, TiN layer, and a bilayer of these material layers.

18. The metal interconnect layer of claim 11, wherein the conductive layer is formed of at least one of a Cu and a W layer.

19. A method for forming a metal interconnect layer of a semiconductor device, the method comprising:

forming an interlevel dielectric (ILD) film over a semiconductor wafer;

forming a photoresist pattern on the ILD film, the photoresist pattern defining a metal interconnect region;

etching a portion of the ILD film using the photoresist pattern as an etch mask to form an initial trench, a polymer layer serving as an etch barrier on the sidewalls of the initial trench;

etching the remainder of the ILD film using the photoresist pattern and the polymer layer on the initial trench sidewalls as an etch mask, to deepen the trench, the resulting deeper trench having a lower width and an upper width, the lower width being wider than the upper width;

removing the photoresist pattern;

forming a barrier layer on the semiconductor wafer and in the deeper trench;

depositing a conductive layer over the barrier layer; and

polishing the conductive layer by chemical mechanical polishing (CMP), such that the conductive layer remains within only the deeper trench.

20. The method of claim 19, wherein, in etching a portion of the ILD film to form the initial trench, a hydrogen containing CF-based gas and an inert gas are used such that the polymer layer is formed on the initial trench sidewalls.

21. The method of claim 19, wherein, in etching the remainder of the ILD film to deepen the trench, a non-hydrogen containing CF-based gas and an inert gas are used together with at least one of oxygen and nitrogen.

22. The method of claim 19, wherein the height of the initial trench with the polymer layer is in the range of 20-70% of the thickness of the entire ILD film.

23. The method of claim 19, wherein the ILD film is formed of at least one of a undoped silicate glass (USG) layer, silicon oxide fluoride (SiOF) layer, tetraethylorthosilicate (TEOS) layer, spin-on glass (SOG) layer and a borophosphosilicate glass (BPSG).

24. The method of claim 19, wherein the barrier layer is formed of at least one of a Ta layer, TaN layer, Ti layer, TiN layer and a bilayer of these layers, acting as both a metal-diffusion barrier and an adhesive layer between the ILD film and the conductive layer.

25. The method of claim 19, wherein the conductive layer is formed of at least one of a Cu and a W layer.

26. A method for forming a metal interconnect layer of a semiconductor device, the method comprising:

forming a first interlevel dielectric (ILD) film over a semiconductor wafer;

forming a second ILD film over the first ILD film, the second ILD film having a lower etch rate than the first ILD film;

forming a photoresist pattern over the second ILD film, the photoresist pattern defining a metal interconnect region;

etching the second ILD film and the first ILD film in sequence using the photoresist pattern as an etch mask, to form a trench having a lower width in the first

ILD film and an upper width in the second ILD film, the lower width being wider than the upper width;

removing the photoresist pattern;

forming a barrier layer along the semiconductor wafer and in the trench;

depositing a conductive layer over the barrier layer; and

polishing the semiconductor wafer with the conductive layer by chemical mechanical polishing such that the conductive layer remains within only the trench surrounded by the first and second ILD films.

27. The method of claim 26, wherein the thickness of the second ILD film is in the range of 20-70% of the sum of the thicknesses of the first and second ILD films.

28. The method of claim 26, wherein the second ILD film is formed of at least one of a undoped silicate glass (USG) layer, silicon oxide fluoride (SiOF) layer, tetraethylorthosilicate (TEOS) layer, spin-on glass (SOG) layer and a borophosphosilicate glass (BPSG); and the first ILD film is formed of at least one of a flowable oxide (FOX) layer and a hydride organic siloxane polymer (HOSP) layer, such that the first ILD film has a higher etch rate than the second ILD film.

29. The method of claim 26, wherein the barrier layer is formed of at least one of a Ta layer, TaN layer, Ti layer, TiN layer and a bilayer of these layers, acting as both a metal-diffusion barrier and an adhesive layer between the ILD film and the conductive layer.

30. The method of claim 26, wherein the conductive layer is formed of at least one of a Cu and a W layer.

31. A method for forming a metal interconnect layer of a semiconductor device, the method comprising the steps of:

(a) forming an interlevel dielectric (ILD) film over a semiconductor wafer;

(b) forming a photoresist pattern on the ILD film, the photoresist pattern defining a metal interconnect region;

(c) etching an upper portion of the ILD film using the photoresist pattern as an etch mask to form an initial trench having a first width, resulting in a polymer layer serving as an etch barrier on the sidewalls of the initial trench;

(d) etching an middle portion of the ILD film using the photoresist pattern and the polymer layer on the initial trench sidewalls as an etch mask, to deepen the trench to form a second portion of the trench, the second portion of the trench having a second width wider than first width of the initial trench;

(e) forming a polymer layer serving as an etch barrier on the lower end of the etched middle portion of the ILD film;

(f) etching the remaining lower portion of the ILD film using the photoresist pattern and the polymer layers on the initial trench sidewalls and the sidewalls of the second portion of the trench as an etch mask, to further deepen the trench to form a third portion of the trench having a third width, the third width being smaller than the second width of the second portion of the trench;

(g) removing the photoresist pattern;

(h) forming a barrier layer along the semiconductor wafer and in the deepened trench;

(i) depositing a conductive layer over the barrier layer; and

(j) polishing the semiconductor wafer with the conductive layer by chemical and mechanical polishing such that the conductive layer remains within only the deepened trench surrounded by the ILD film.

32. The method of claim 31, wherein, in steps (c) and (e), a hydrogen containing CF-based gas and an inert gas are used to cause the polymer layer on the initial trench sidewalls and the lower end of the second portion of the trench.

33. The method of claim 31, wherein, in steps (d) and (f), a non-hydrogen containing CF-based gas and an inert gas are used together with at least one of oxygen and nitrogen.

34. The method of claim 31, wherein the thickness of the middle portion of the ILD film is in the range of 20-50% of the thickness of the entire ILD film.

35. The method of claim 31, wherein the ILD film is formed of at least one of a undoped silicate glass (USG) layer, silicon oxide fluoride (SiOF) layer, tetraethylorthosilicate (TEOS) layer, spin-on glass (SOG) layer and a borophosphosilicate glass (BPSG).

36. The method of claim 31, wherein the barrier layer is formed of at least one of a Ta layer, TaN layer, Ti layer, TiN layer and a bilayer of these layers, acting as both a metal-diffusion barrier and an adhesive layer between the ILD film and the conductive layer.

37. The method of claim 31, wherein the conductive layer is formed of at least one of a Cu and a W layer.

38. A method for forming a metal interconnect layer of a semiconductor device, the method comprising:

forming a first interlevel dielectric (ILD) film over a semiconductor wafer;

forming a second ILD film over the first ILD film, the second ILD film having a higher etch rate than the first ILD film;

forming a third ILD film over the second ILD film, the third ILD film having a lower etch rate than the second ILD film;

forming a photoresist pattern over the third ILD film, the photoresist pattern defining a metal interconnect region;

etching the third ILD film, the second ILD film, and the first ILD film in sequence using the photoresist pattern as an etch mask, to form a trench having a lower width, a middle width and an upper width, the middle width in the second ILD film being wider than the upper width in the third ILD film and the lower width in the first ILD film;

removing the photoresist pattern;

forming a barrier layer along the semiconductor wafer and in the trench;

depositing a conductive layer over the barrier layer; and

polishing the semiconductor wafer with the conductive layer by chemical mechanical polishing such that the conductive layer remains within only the trench surrounded by the first, second and third ILD films.

39. The method of claim 38, wherein the thickness of the second ILD film is in the range of 20-50% of the sum of the thicknesses of the first, second and third ILD films.

40. The method of claim 38, wherein each of the first and third ILD films is formed of at least one of an undoped silicate glass (USG) layer, silicon oxide fluoride (SiOF) layer, tetraethylorthosilicate (TEOS) layer, spin-on glass (SOG) layer and a borophosphosilicate glass (BPSG); and the second ILD film is formed of at least one of a flowable oxide (FOX) layer and a hydride organic siloxane polymer (HOSP) layer such that the second ILD film has a higher etch rate than the first and third ILD films.

41. The method of claim 38, wherein the barrier layer is formed of at least one of a Ta layer, TaN layer, Ti layer, TiN layer and a bilayer of these layers, acting as both a metal-diffusion barrier and an adhesive layer between the first, second and third ILD films, and the conductive layer.

42. The method of claim 38, wherein the conductive layer is formed of at least one of a Cu and a W layer.